DATA SHEET

LXK6712E: 5 GHz WLAN Front End Module for 802.11ac

Applications

- IEEE 802.11a/n/ac wireless LAN system
- 5GHz ISM Band application
- WiFi-enabled wireless portable systems

Features

- Integrated 5GHz PA, LNA with bypass and SPDT
- Transmit gain: 30dB
- Receive gain: 15 dB
- 50 Ohm input and output impedance
- Output power: 19dBm@1.8% EVM, 11ac, HT80,MCS9
- Temperature compensation
- Small QFN (16-pin, 3mm x 3mm) package

Product Description

The LXK6712E is a highly integrated front end module (FEM) including a 5 GHz Power amplifier, an LNA with bypass and a SPDT Transmit/Receive switch. It is intended for 802.11a/n/ac wireless LAN applications. A digital enable/disable function is included in both PA and LNA which allows power saving during off mode.

The LXK6712E is housed in a miniature 16-pin, 3mm x 3mm QFN package.A functional block diagram is shown in Figure1. A package and pin-out view of LXK6712E is shown in Figure 2.

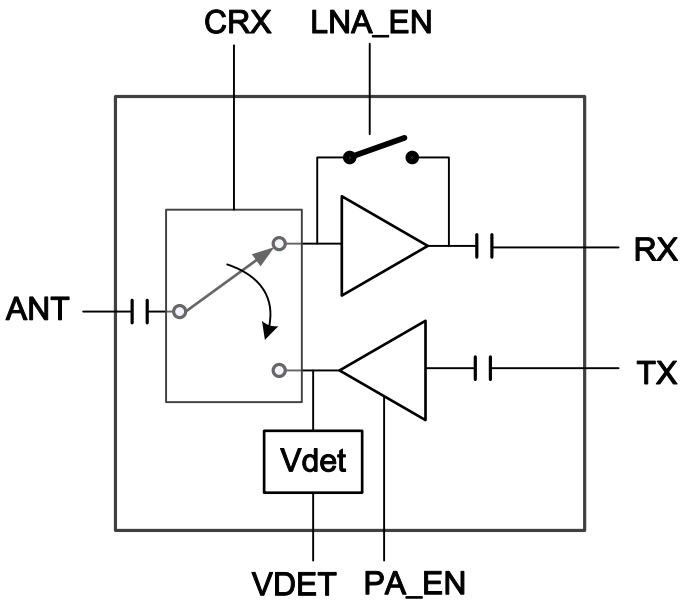


Figure 1. LXK6712E Functional Block Diagram

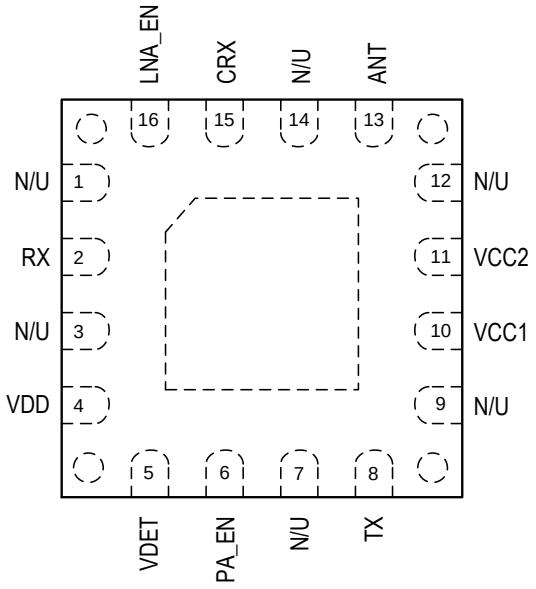


Figure 2. LXK6712E Pinout – 16-Pin QFN

Table 1. LXK6712E Signal Description

Pin#	Name	Description	Pin#	Name	Description
1	N/U	No connection	9	N/U	No connection
2	RX	RF receiver output	10	VCC1	PA supply voltage 1
3	N/U	No connection	11	VCC2	PA supply voltage 2
4	VDD	LNA supply voltage	12	N/U	No connection
5	VDET	Power detector output	13	ANT	Antenna port
6	PA_EN	PA enable control	14	N/U	No connection
7	N/U	No connection	15	CRX	Switch control voltage
8	TX	RF transmitter input	16	LNA_EN	LNA enable control

Table 2 Absolute Maximum Rating

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	VCC1,VCC2	-0.3	+6.0	V
Supply voltage	VDD		+6.0	V
DC input on control pins (PA_EN, LNA_EN, CRX)	V_{IN}	-0.3	+3.6	V
Input power (50 Ω load)	P_{IN}		+10	dBm
Supply current	I_{CC}		500	mA
Storage temperature	T_{STG}	-40	+150	℃
Operating ambient temperature	T_{op}	-40	+85	℃
Junction temperature	T_J		150	℃
ESD Rating – Human Body Model	ESD		Class 1C	

Table 3.Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
PA supply voltage	VCC1,VCC2	4.5	5.0	5.5	V
LNA supply voltage	VDD	4.5	5.0	5.5	V
PA supply current	I_{CC}		300		mA
LNA supply current	I_{DD}		14		mA
Control logic: High Low	 V_{HI} V_{LO}	 2.5 0		 3.6 0.2	 V V
PA enable current (PA_EN high)	I_{PA_EN}		20		uA
LNA enable current(LNA_EN high)			140		uA
CRX enable current			40		uA

Note 1:The minimum voltage for CRX logic high is 2.0V.

Table 4 Control Logic

Mode	State	CRX	LNA_EN(note1)	PA_EN
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	1	0
WLAN receive bypass	3	1	0	0
WLAN transmit	4	0	0	1

Note 1:LNA is on while LNA_EN is high. LNA is off and in bypass mode when LNA_EN is low.

Table 5. Electrical Specifications (TA=+25℃)

Parameters			Minimu	Typical	Maxim	Units
Transmit Characteristics (Vcc=+5.0V, PA_EN=3.0V, LNA_EN=CRX=0V)						
Frequency			5150		5850	MHz
Small signal gain			27	30	33	dB
Gain flatness over band（over any 40MHz bandwidth）			-0.5		+0.5	dB
Input return loss(|S11|)			12	15		dB
Output return loss(|S22|)			7	10		
Isolation (Ant port to RX port)				40		dB
Pout	IEEE802.11a	54 Mbps, 64 QAM，-30dB EVM	19	21		dBm
		6Mbps，Mask compliant	22	24		
	IEEE802.11n	HT20，MCS7，-30dB EVM	19	21		
		HT20，MCS0，Mask compliant	21	23		
	IEEE802.11ac	HT40，MCS9，-35dB DEVM	18	20		
		HT40，MCS0，Mask compliant	21	23		
		HT80，MCS9，-35dB DEVM	17	19		
		HT80，MCS0，Mask compliant	20	22		
Harmonics (Pout=22dBm,MCS0)		2^{nd}		-8		dBm/MHz
		3^{rd}		-45		
PA switching time (50% of VPA_EN edge and 90/10% of final output power level)				130	200	ns
Quiescent supply current Icq				300		mA
Operating supply current, Pout=20dBm				360		mA
Stability	CW, POUT =+20 dBm, 0.1 GHz to 20 GHz, loadVSWR = 6:1		All non-harmonically related outputs < －42dBm/MHz			
Ruggedness	CW, PIN = =8 dBm, 0.1 GHz to20 GHz, load VSWR = 10:1		No permanent damage or performance degradation			
Receive Characteristics (VDD=+5.0V, PA_EN=0V, LNA_EN=CRX=3.3V)						
Frequency			5150		5850	MHz
Small signal gain			13	15	17	dB
Gain flatness over band（over any 40MHz bandwidth）			-0.5		+0.5	dB
Input return loss(|S11|)			7	10		dB
Output return loss(|S22|)			5	8		dB
Isolation (Ant port to TX)				40		dB
3^{rd} order Input Intercept Point IIP3				-3		dBm
1dB Input Compression Point IP1dB				+9		dBm
Noise Figure				2.3	2.6	dB
Supply current, RX On				14		mA
Enable time				500	600	ns
Receive Bypass Characteristics						
Insertion loss |S21|				-7		dB
1dB Input Compression Point IP1dB				+8		dBm

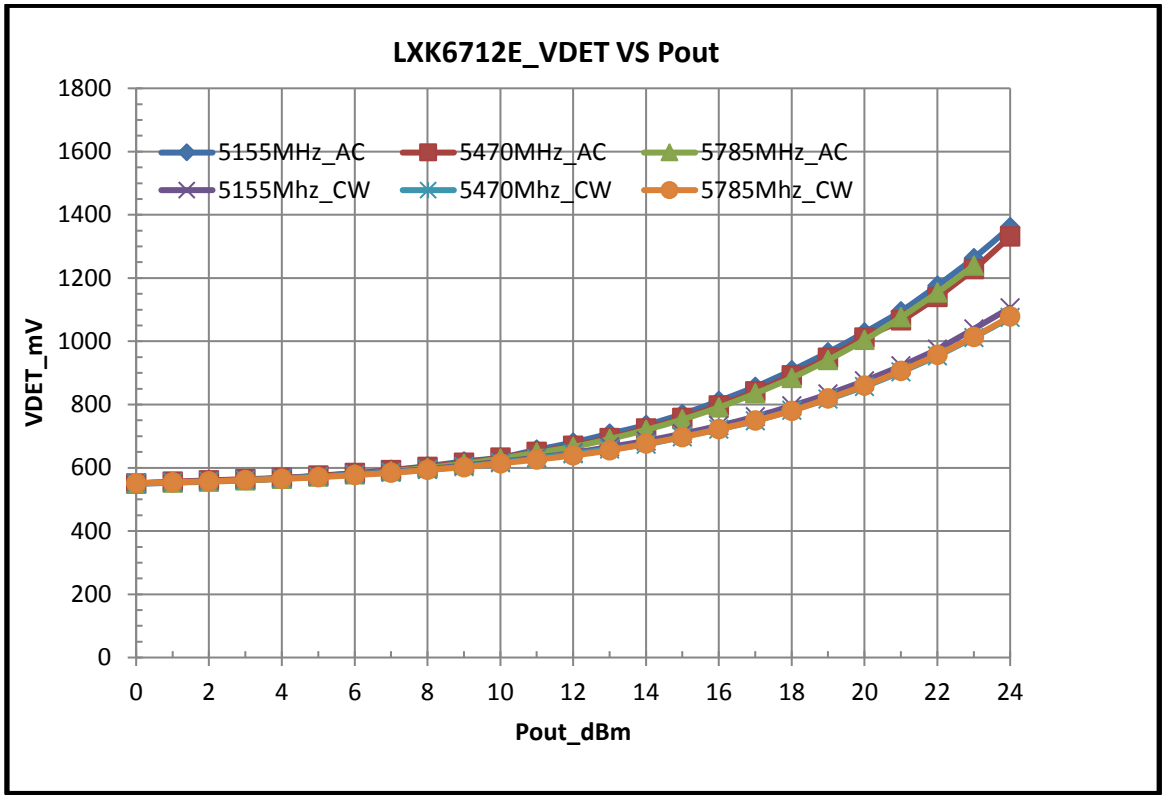


Figure 3.LXK6712E Detector Characteristics

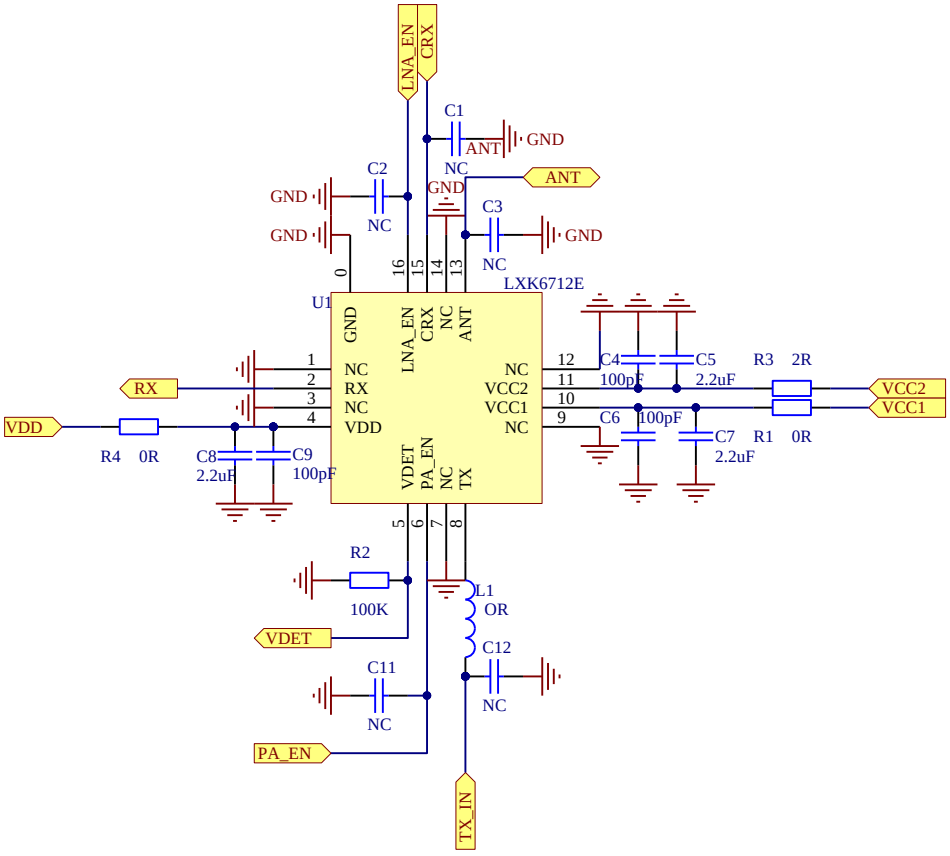


Figure 4.LXK6712E Application Schematic

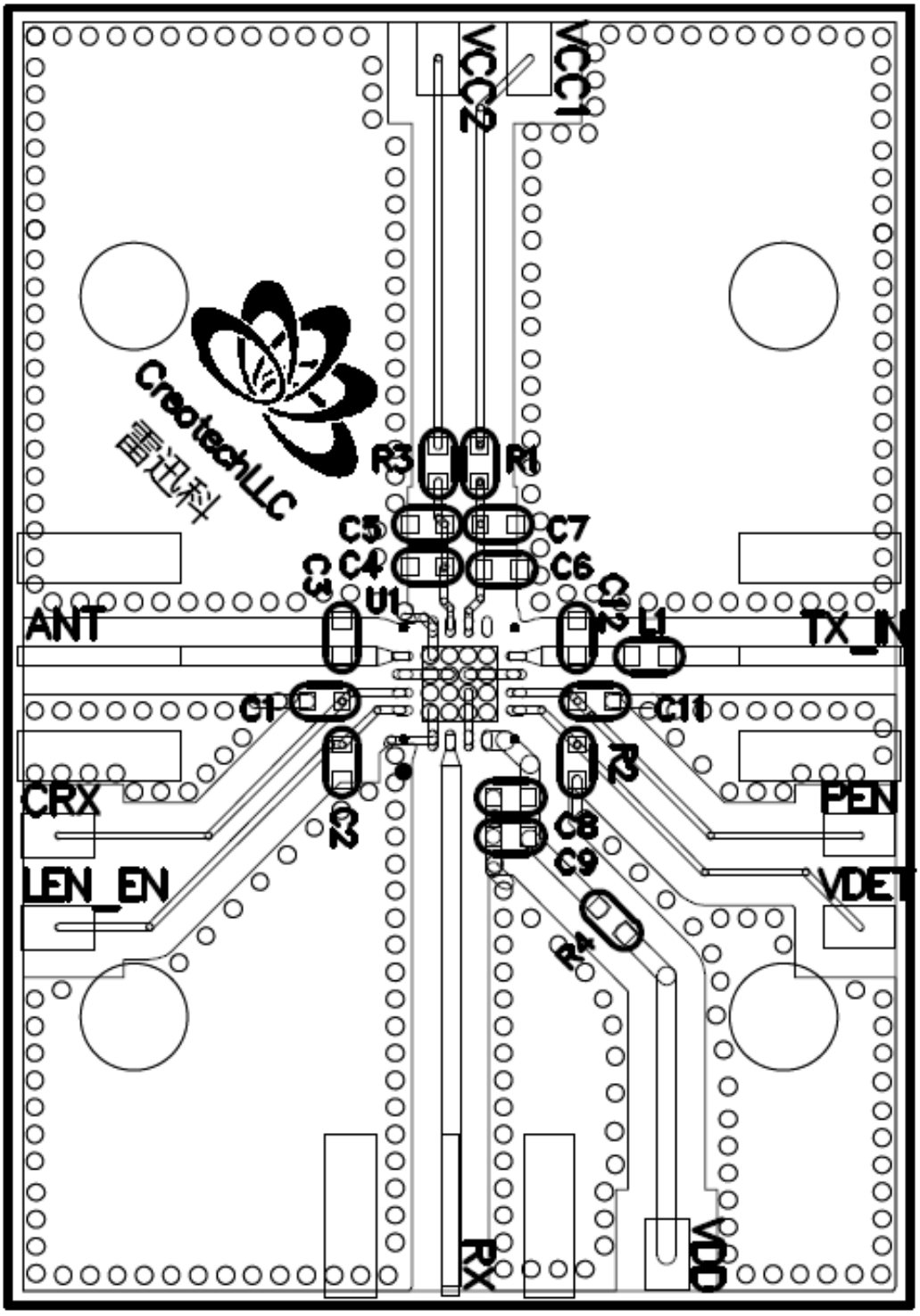
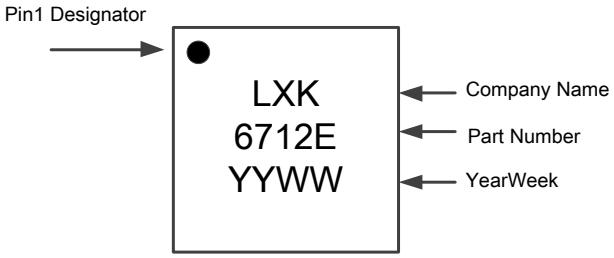
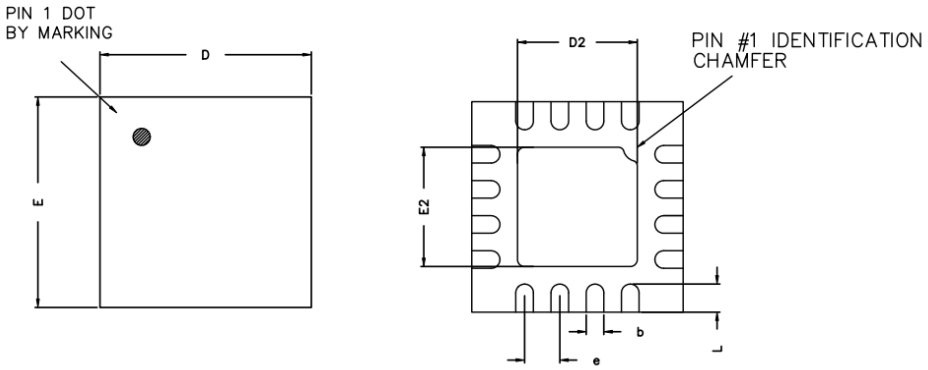


Figure 5. LXK6712E Evaluation Board Assembly Drawing

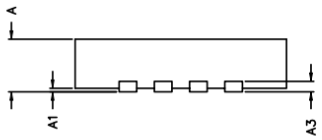
Package diagram:





TOP VIEW

BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.18	0.25	0.30
L	0.20	0.30	0.40
D2	1.55	1.70	1.80
E2	1.55	1.70	1.80
e	0.5 BSC		

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
LXK6712EFEM	LXK6712E	EVB-LXK6712E-01

Document Change History

Revision	Date	Notes
1.0	Oct. 20, 2017	Created.
1.0	Jul. 31, 2018	Update.